REMARKS

The Office Action of **July 1, 2002**, has been received and its contents carefully noted. Applicant respectfully submits that this response is timely filed and fully responsive to the Office Action.

Claims 1-27 were pending in the present application prior to the above amendment, with claims 10-27 being withdrawn from consideration. By the above amendment, claims 1 and 3-9 amended and new claims 28-38 added. Applicant submits that no issue of new matter is set forth by the aforementioned amendment. For instance amended claim 1 is based on Fig. 1A and page 6, line 20 through page 7, line 11 of the present specification; amended claim 6 is based on Fig. 6A; new claim 32 is based on page 27, lines 15-21 of the present specification; new claim 34 is based on page 28, lines 9-14 of the present specification; and new claim 38 is based on page 49, lines 6-11 of the present specification. Accordingly, claims 1-38 are presently pending in the subject application, of which claims 1-9 and 28-38 are allowable over the prior art for at least the reasons advanced below.

A. OBJECTION TO THE SPECIFICATION

The disclosure is objected to as containing various informalities. In response thereto, the disclosure has been amended in the manner suggested by the Examiner. Moreover, the title of the invention is replaced with one which is indicative of the invention to which the claims are directed. Specifically, the new title of the invention is "Semiconductor Device Having Diffusion Layer Formed Using Dopant of Large Mass Number." Accordingly, withdrawal of the objections is respectfully requested.

B. OBJECTION TO THE CLAIMS

Claims 4 and 8 are objected to as containing various informalities. In response thereto, claims 4 and 8 are amended so as to remove the phrase "heavily-doped" therefrom. Accordingly, withdrawal of the objection is respectfully requested.

C. 35 U.S.C. 102 REJECTION

Claim 1 stands rejected under 35 U.S.C. §102(e) as anticipated by U.S. Patent No. 6,093,951 to Burr and claims 1 and 3 stand rejected under 35 U.S.C. §102(e) as anticipated by U.S. Patent No. 6,063,682 to Sultan et al. ("Sultan"). Applicant respectfully contends that the claimed subject matter as presently amended clearly defines over the cited references for at least the following reasons.

1. Summary of the Invention

Amended claim 1 of the present invention is directed generally to a semiconductor device comprising an epitaxial semiconductor substrate having an epitaxial region of silicon included in at least an upper portion thereof; and a diffusion layer formed in said epitaxial region by using a dopant ion having a relatively large mass number, wherein said diffusion layer is formed shallower than said epitaxial region.

2. Burr Fails to Teach the Claimed Invention

Burr teaches implanting an indium ion as a dopant ion having a relatively large mass number into a pocket region of a MOS device (column 14, lines 35-41), and forming the pocket

region extending into a bulk region (column 5, lines 48-49). Burr also teaches at column 16, lines 6-9 forming an epitaxial silicon layer serving as a channel region after the pocket implantation. Thus, the invention of Burr is different from that of amended claim 1 insofar as claim 1 requires that the diffusion layer is formed in the expitaxial region. Moreover, Burr fails to teach or suggest forming the pocket region in the epitaxial silicon layer. Accordingly, withdrawal of the rejection is respectfully requested.

3. Sultan Fails to Teach the Claimed Invention

Sultan teaches a step of forming an amorphous portion in a silicon substrate by ion implanting indium ion, having a relatively large mass number, into the substrate. Column 6, lines 24-30. Hence, since the ion implanted amorphous portion is formed in the silicon substrate, the invention of Sultan is different from that of the amended claim 1 of the present invention, which requires forming the diffusion layer in the expitaxial region.

Moreover, Sultan teaches at column 7, lines 10-12 that the epitaxial region asserted by the Examiner is a region of "solid phase epitaxial growth," which is completely different from the epitaxial region of the amended claim 1 that is formed by epitaxial growth. As described in column 7, lines 10-12 of Sultan, the "solid phase epitaxial growth" is merely a phenomenon of crystal recovery of the amorphous portion along the plane orientation of the substrate, in the step of a re-crystallization of the amorphous portion, which is amorphized by ion implantation under a temperature range of 550°C-650°C. Further, Sultan discloses in Fig. 2a, "AMORPHOUS REGION" and "CRYSTALLIN REGION," but fails to disclose the epitaxial region of the claimed invention. Accordingly, the claimed invention as presently amended is clearly

patentably distinct from the Sultan patent. Accordingly, withdrawal of the rejection is respectfully requested.

D. 35 U.S.C. 103 REJECTION

Claim 3 stands rejected under 35 U.S.C. §103(a) as unpatentable over Burr, claim 2 stands rejected under 35 U.S.C. §103(a) as unpatentable over Burr in view of U.S. Patent No. 5,177,569 to Koyama, and claims 4-9 stand rejected under 35 U.S.C. §103(a) as unpatentable over the alleged Admitted Prior Art (APA) in view of Burr and Koyama.

1. Summary of the Invention

As previously stated in response to the §102 rejection, independent claim 1 is amended to recite a semiconductor device comprising an epitaxial semiconductor substrate having an epitaxial region of silicon included in at least an upper portion thereof; and a diffusion layer formed in said epitaxial region by using a dopant ion having a relatively large mass number, wherein said diffusion layer is formed shallower than said epitaxial region. Dependent claims 2-5 incorporate by reference such features since they are dependent on claim 1.

Such combination of features are non-obviously advantageous since the epitaxial semiconductor substrate has an expitaxial region of silicon included in at least the upper portion thereof is used as a semiconductor substrate. Hence, as described in page 26, lines 3-9 of the present specification, the occurrence of EOR dislocation loop defects in the diffusion layer formed in the expitaxial region by using the dopant ions composed of heavy ions can be suppressed as compared to a semiconductor substrate prepared by the general CZ method. As a

result, heavy ions are minimally segregated in a region below an amorphous-crystal interface which is produced during the implantation of the heavy ions, and hence, the semiconductor device can be refined with a leakage current derived from the segregation suppressed.

Independent claim 6 is amended recite generally a semiconductor device comprising a semiconductor substrate composed of silicon and having a main surface of a {110} orientation, and a diffusion layer formed by using a dopant ion having a relatively large mass number in the semiconductor substrate. Dependent claims 7-9 incorporate by reference such features since they are dependent on claim 6.

Such combination of features are non-obviously advantageous since the semiconductor device uses a semiconductor substrate having a {110} orientation, and thus, a {110} oriented zone axis. Hence, the implanted heavy ion is channeled to result in fewer collision with the silicon atom, resulting in reduced implantation damage to the semiconductor substrate. Consequently, formation of interstitial silicon is suppressed and EOR dislocation loop defects are less likely to occur so that the heavy ions can be minimally segregated in the region below the original amorphous-crystal interface. Therefore, a leakage current derived from the segregation suppressed. Moreover, even though heavy ions are channeled due to the mass of the heavy ions, the implanting range will not be bigger than that of light ions, and thus, a shallow junction can be achieved.

2. The Cited References Fail to Disclose the Claimed Invention

As previously stated in response to the §102 rejection, the claimed subject matter of the present invention is patentably distinct from the Burr device insofar as Burr lacks the formation

of the diffusion layer in the expitaxial region. Moreover, Burr fails to teach or suggest forming the pocket region in the epitaxial silicon layer. As a result, the non-obvious benefits derived from the claimed invention cannot be achieved by Burr. Namely, the semiconductor device disclosed by Burr does not suppress the occurrence of EOR dislocation loop defects in the diffusion layer formed in the expitaxial region by using the dopant ions composed of heavy ions. Accordingly, withdrawal of the rejection is respectfully requested in view of the foregoing remarks.

Regarding the rejection of claims 6-9, as conceded by the Examiner, the alleged APA fails to disclose a semiconductor substrate having a {110} orientation. Koyama teaches, for example, in Fig. 2, Fig. 4A and column 6, lines 63-68, the plane orientations of a polycrystal silicon layer 4 and a single crystal silicon layer 5, both composed of gate electrode 10. Hence, Koyama merely discloses a {110} orientation of the gate electrode, and thus, not a semiconductor substrate having a {110} orientation. Hence, there is no motivation to combine Koyama with the alleged APA insofar as the gate electrode is generally not formed in the diffusion layer formed by ion implantation.

As a result, the non-obvious benefits derived from the claimed invention cannot be achieved by the proposed combination of references. In particular, the proposed combination of references does not result in reduced implantation damage to the semiconductor substrate, the suppression of the formation of interstitial silicon, and a reduction in the occurrence of EOR dislocation loop defects.

Moreover, as described above, since Burr merely disclose implanting an indium ion as a dopant ion having a relatively large mass number into a pocket region of a MOS device, the amended claim 6 (and dependent claims 7-9) of the present invention is patentable over the

proposed combination of Burr, Koyama and the alleged APA. Withdrawal of the rejection is respectfully requested in view of the foregoing remarks.

CONCLUSION

Having responded to all rejections set forth in the outstanding non-Final Office Action, it is submitted that claims 1-9 and 28-38 are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,

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IN THE CLAIMS:

1. (Amended) A semiconductor device comprising:

an epitaxial semiconductor substrate having an expitaxial region of silicon included in at least an upper portion thereof; and

a [heavily-doped] diffusion layer formed in said expitaxial region, by using a dopant ion having a relatively large mass number, [in an epitaxial region of silicon included in at least an upper portion of an epitaxial semiconductor substrate]

wherein said diffusion layer is formed shallower than said epitaxial region.

3. (Amended) The semiconductor device of Claim 1,

wherein said [heavily-doped] diffusion layer is formed by using, as said dopant ion, an indium ion [at a dose of $5 \times 10^{13}/cm^{-2}$ or more].

4. (Amended) The semiconductor device of Claim 1,

wherein said [heavily-doped] diffusion layer corresponds to a pocket [heavily-doped] diffusion layer of a MIS semiconductor device, and

said MIS semiconductor device includes:

a gate electrode formed above said epitaxial region with a gate insulating film sandwiched therebetween;

a source/drain [heavily-doped] diffusion layer of a first conductivity type formed in a source/drain region of said epitaxial region at a distance from a region below a side face of said gate electrode;

an extension [heavily-doped] diffusion layer of the first conductivity type formed in said epitaxial region between said source/drain [heavily-doped] diffusion layer and said region below the side face of said gate electrode and having shallower junction than said source/drain [heavily-doped] diffusion layer; and

said pocket [heavily-doped] diffusion layer of a second conductivity type formed in said epitaxial region under said extension [heavily-doped] layer.

5. (Amended) The semiconductor device of Claim 4,

wherein said extension [heavily-doped] diffusion layer is formed by using an antimony ion as a dopant.

6. (Amended) A semiconductor device comprising:

a semiconductor substrate composed of silicon and having a main surface of {110}-orientation; and

a [heavily-doped] diffusion layer formed, by using a dopant ion having a relatively large mass number, in [a] said semiconductor substrate [having a <110>-oriented zone axis].

7. (Amended) The semiconductor device of Claim 6.

wherein said [heavily-doped] diffusion layer is formed by using, as said dopant ion, an indium ion [at a dose of 5 X $10^{13}/cm^{-2}$ or more].

8. (Amended) The semiconductor device of Claim 6,

wherein said [heavily-doped] diffusion layer corresponds to a pocket [heavily-doped] diffusion layer of a MIS semiconductor device, and

said MIS semiconductor device includes:

a gate electrode formed above said semiconductor substrate with a gate insulating film sandwiched therebetween;

a source/drain [heavily-doped] diffusion layer of a first conductivity type formed in a source/drain region of said semiconductor substrate at a distance from a region below a side face of said gate electrode;

an extension [heavily-doped] diffusion layer of the first conductivity type formed in said semiconductor substrate between said source/drain [heavily-doped] diffusion layer and said region below the side face of said gate electrode and having shallower junction than said source/drain [heavily-doped] diffusion layer; and

said pocket [heavily-doped] diffusion layer of a second conductivity type formed in said semiconductor substrate under said extension [heavily-doped] diffusion layer.

9. (Amended) The semiconductor substrate of Claim 8,

wherein said extension [heavily-doped] diffusion is formed by using an antimony ion as a dopant.

IN THE SPECIFICATION:

On page 3, please replace the first full paragraph with the following substitute paragraph.

--Next, as shown in FIG. 8D, with the gate electrode 103 and the sidewall 106 used as a mask, As ions, that is, an N-type dopant, are implanted into the semiconductor substrate 101 at acceleration energy of 30 keV and a dose of approximately 3 x $10^{15}/cm^2$, and then annealing is carried out at a high temperature for a short period of time. Thus, an N-type source/drain heavily-doped diffusion layer 107 with deep junction is formed in the source/drain region of the semiconductor substrate 101, an N-type extension region heavily-doped diffusion layer 105B with shallower junction than the source/drain heavily-doped diffusion layer 107 is formed on the inside of the source/drain heavily-doped diffusion layer 107, and a P-type pocket region of heavily-doped diffusion layer 104B is formed under the extension region heavily-doped diffusion layer 105B.--

On page 4, please replace the final paragraph abridging pages 4 and 5 with the following substitute paragraph.

--In particular, in the dopant implantation using heavy ions, the amorphous-crystal interface is formed in a position deeper than the concentration peek of the dopant, and hence, the junction plane obtained after diffusion of the extension heavily-doped diffusion layer 105B is formed in a position deeper than a designed depth. Furthermore, when the EOR dislocation loop defect layer is formed in the vicinity of the junction plane of the extension region of heavily-doped diffusion layer 105B, junction leakage is disadvantageously caused.--

On page 7, please replace the final paragraph abridging pages 7 and 8 with the following substitute paragraph.

--In the first semiconductor device, the heavily-doped diffusion layer preferably corresponds to a pocket region of heavily-doped diffusion layer of a MIS semiconductor device, and the MIS semiconductor device preferably includes a gate electrode formed above the epitaxial region with a gate insulating film sandwiched therebetween; a source/drain heavily-doped diffusion layer of a first conductivity type formed in a source/drain region of the epitaxial region at a distance from a region below a side face of the gate electrode; an extension region heavily-doped diffusion layer of the first conductivity type formed in the epitaxial region between the source/drain heavily-doped diffusion layer and the region below the side face of the gate electrode and having shallower junction than the source/drain heavily-doped diffusion layer; and the pocket region of heavily-doped diffusion layer of a second conductivity type formed in the epitaxial region under the extension heavily-doped diffusion layer. In this manner, the pocket region of heavily-doped diffusion layer is formed from the heavily-doped diffusion layer of this invention, and hence, the extension region heavily-doped diffusion layer and the pocket region of heavily-doped diffusion layer formed between the source/drain heavily-doped diffusion layers can attain shallow junction.--

On page 8, please replace the final full paragraph with the following substitute paragraph.

--In this case, the extension region heavily-doped diffusion layer is preferably formed by using an antimony ion as a dopant. In this manner, since an antimony ion is an N-type heavy ion, the junction depth of the extension region heavily-doped diffusion layer can also definitely attain

shallow junction.--

On page 9, please replace the final paragraph abridging pages 9 and 10 with the following substitute paragraph.

--In the second semiconductor device, the heavily-doped diffusion layer preferably corresponds to a pocket heavily-doped diffusion layer of a MIS semiconductor device, and the MIS semiconductor device preferably includes a gate electrode formed above the semiconductor substrate with a gate insulating film sandwiched therebetween; a source/drain heavily-doped diffusion layer of a first conductivity type formed in a source/drain region of the semiconductor substrate at a distance from a region below a side face of the gate electrode; an extension region heavily-doped diffusion layer of the first conductivity type formed in the semiconductor substrate between the source/drain heavily-doped diffusion layer and the region below the side face of the gate electrode and having shallower junction than the source/drain heavily-doped diffusion layer; and the pocket region of heavily-doped diffusion layer of a second conductivity type formed in the semiconductor substrate under the extension heavily-doped diffusion layer.--

On page 10, please replace the first full paragraph with the following substitute paragraph.

--In this case, the extension region heavily-doped diffusion layer is preferably formed by using an antimony ion as a dopant.--

On page 10, please replace the third full paragraph with the following substitute paragraph.

--Since a pocket region of heavily-doped diffusion layer is formed by implantation and diffusion of the dopant heavy ion in the epitaxial region of silicon in the first method for fabricating a semiconductor device, the heavy ion is minimally segregated in the region below the original amorphous-crystal interface. Accordingly, the semiconductor device can be refined with a leakage current derived from the segregation suppressed.--

On page 11, please replace the second full paragraph with the following substitute paragraph.

--In the first method for fabricating a semiconductor device, the heavily-doped diffusion layer is preferably formed by using, as the dopant ion, an indium ion at a dose of $5 \times 10^{3}/cm^{2}$ or more. Since the first dopant layer can be thus changed into an amorphous layer, the channeling of the second dopant subsequently implanted can be suppressed. Accordingly, the extension region heavily-doped diffusion layer and the pocket region of heavily-doped diffusion layer can definitely attain shallow junction, resulting in realizing a semiconductor device with high driving power.--

On page 11, please replace the final paragraph abridging pages 11 and 12 with the following substitute paragraph.

--In the first method for fabricating a semiconductor device, the heavily-doped diffusion layer preferably corresponds to a pocket region of heavily-doped diffusion layer of a MIS

semiconductor device, and the method for fabricating the MIS semiconductor device preferably includes the steps of forming a gate electrode above the epitaxial region with a gate insulating film sandwiched therebetween; forming a first dopant layer to be used as the pocket region of heavily-doped diffusion layer by implanting a first dopant of a first conductivity type corresponding to the dopant ion into the epitaxial region with the gate electrode used as a mask; forming a second dopant layer to be used as an extension region heavily-doped diffusion layer by implanting a second dopant of a second conductivity type into the epitaxial region to have shallower junction than the first dopant layer with the gate electrode used as a mask; and forming a sidewall on a side face of the gate electrode, and forming a third dopant layer to be used as a source/drain heavily-doped diffusion layer by implanting a third dopant of the second conductivity type into the epitaxial region to have deeper junction than the second dopant layer with the gate electrode and the sidewall used as a mask. In this manner, the extension region heavily-doped diffusion layer formed between the source/drain heavily-doped diffusion layers and the pocket region of heavily-doped diffusion layer formed under the extension region heavily-doped diffusion layer can attain shallow junction.--

On page 14, please replace the final paragraph abridging pages 14 and 15 with the following substitute paragraph.

--In the second method for fabricating a semiconductor device, the heavily-doped diffusion layer preferably corresponds to a pocket heavily-doped diffusion layer of a MIS semiconductor device, and the method for fabricating the MIS semiconductor device preferably includes the steps of forming a gate electrode above the semiconductor substrate with a gate

insulating film sandwiched therebetween; forming a first dopant layer to be used as the pocket region of heavily-doped diffusion layer by implanting a first dopant of a first conductivity type corresponding to the dopant ion into the semiconductor substrate with the gate electrode used as a mask; forming a second dopant layer to be used as an extension region heavily-doped diffusion layer by implanting a second dopant of a second conductivity type into the semiconductor substrate to have shallower junction than the first dopant layer with the gate electrode used as a mask; and forming a sidewall on a side face of the gate electrode, and forming a third dopant layer to be used as a source/drain heavily-doped diffusion layer by implanting a third dopant of the second conductivity type into the semiconductor substrate to have deeper junction than the second dopant layer with the gate electrode and the sidewall used as a mask.--

On page 16, please replace the final paragraph abridging pages 16 and 17 with the following substitute paragraph.

--In the third method for fabricating a semiconductor device, the heavily-doped diffusion layer preferably corresponds to a pocket region of heavily-doped diffusion layer of a MIS semiconductor device, and the method for fabricating the MIS semiconductor device preferably includes the steps of forming a gate electrode above the semiconductor substrate with a gate insulating film sandwiched therebetween; forming a first dopant layer to be used as the pocket region of heavily-doped diffusion layer by implanting a first dopant of a first conductivity type corresponding to the dopant ion into the semiconductor substrate with the gate electrode used as a mask; forming a second dopant layer to be used as an extension region heavily-doped diffusion layer by implanting a second dopant of a second conductivity type into the semiconductor

substrate to have shallower junction than the first dopant layer with the gate electrode used as a mask; and forming a sidewall on a side face of the gate electrode, and forming a third dopant layer to be used as a source/drain heavily-doped diffusion layer by implanting a third dopant of the second conductivity type into the semiconductor substrate to have deeper junction than the second dopant layer with the gate electrode and the sidewall used as a mask.--

On page 19, please replace the final paragraph with the following substitute paragraph.

--In an upper portion of the epitaxial semiconductor substrate 11, source/drain heavily-doped diffusion layers 17 where N-type arsenic (As) ions are diffused are formed in source/drain regions positioned on both sides of a sidewall 16 of the gate electrode 13 at a distance from a region below each side face of the gate electrode 13. An extension heavily-doped diffusion layer 15 where N-type As ions are diffused so as to have shallower junction than the source/drain heavily-doped diffusion layer 17 is formed between the source/drain heavily-doped diffusion layer 17 and the region below the side face of the gate electrode 13. A pocket region of heavily-doped diffusion layer 14 where P-type indium (In) ions, that is, heavy ions with a relatively large mass number, are diffused is formed under the extension region heavily-doped diffusion layer 15. Also, a channel diffusion layer 11a where P-type In ions are diffused is formed in a region under the gate electrode 13 in the epitaxial semiconductor substrate 11 sandwiched between the extension region heavily-doped diffusion layers 15 and between the pocket region of heavily-doped diffusion layers 14.--

On page 20, please replace the first paragraph with the following substitute paragraph.

--In this manner, the MIS transistor of this embodiment is characterized by including the pocket region of heavily-doped diffusion layer 14 formed by diffusing the In ions, that is, the heavy ions, in the epitaxial semiconductor substrate 11.--

On page 20, please replace the second paragraph with the following substitute paragraph.

--In FIG. 1B, a curve 1A indicates an As ion concentration in the extension region heavily-doped diffusion layer 15, and a curve 2A indicates an In ion concentration in the pocket region of heavily-doped diffusion layer 14. A broken curve 3 indicates, as a comparison, an In ion concentration in a pocket region of heavily-doped diffusion layer formed by using a silicon wafer prepared by a general rotational pulling (CZ) method as the semiconductor substrate.--

On page 20, please replace the final paragraph abridging pages 20 and 21 with the following substitute paragraph.

--In the semiconductor fabrication process, a heavy ion having a relatively large mass number, such as an In ion, exhibits abrupt implantation profile as compared with an ion having a relatively small mass number such as a boron (B) ion. In addition, as shown in FIG. 1B, the heavy ions are less diffused in a tale portion with a low concentration in the dopant profile, namely, in a deep region, owing to segregation in a defect layer or surface diffusion. Therefore, an abrupt profile can be realized in not only the curve 1A of the dopant concentration in the extension region heavily-doped diffusion layer 15 but also the curve 2A of the dopant concentration in the pocket region of heavily-doped diffusion layer 14. As a result, even in a MIS transistor with a small gate length, shallow junction can be obtained, so as to realize high driving power. Furthermore, since the extension region heavily-doped diffusion layer 15 and the pocket

region of heavily-doped diffusion layer 14 can attain shallow junction, the short channel effect can be suppressed, and hence, a fine transistor can be designed.--

On page 21, please replace the first paragraph with the following substitute paragraph.

--Also, as understood from FIG. 13, since the epitaxial semiconductor substrate 11 is used as the semiconductor substrate in this embodiment, occurrence of EOR dislocation loop defects is reduced in the dopant curve 2A of the pocket region of heavily-doped diffusion layer 14 of this embodiment as compared with that in the dopant curve 3 of the pocket region of heavily-doped diffusion layer formed in the semiconductor substrate prepared by the conventional CZ method. As a result, the peak of the segregation of the In ions in the EOR dislocation loop defect layer can be lowered. Accordingly, a leakage current derived from the heavy ions segregated in the EOR dislocation loop defect layer can be suppressed.--

On page 22, please replace the final paragraph abridging pages 22 and 23 with the following substitute paragraph.

--Next, as shown in FIG. 2B with the gate electrode 13 used as a mask, P-type dopant ions such as In ions are implanted into the epitaxial semiconductor substrate 11 at an acceleration energy of approximately 30 keV and a dose of approximately $1 \times 10^{14}/cm^2$. Then, with the gate electrode 13 used as a mask, N-type dopant ions such as As ions are implanted into the epitaxial semiconductor substrate 11 at an acceleration energy of approximately 10 keV and a dose of approximately $5 \times 10^{14}/cm^2$. Thereafter, the rapid thermal annealing for increasing the temperature at a rate of approximately 100°C/sec. to a high temperature of approximately 900°C

through 1025°C and keeping the temperature for approximately 1 through 10 seconds is carried out. Thus, P-type pocket region of heavily-doped diffusion forming layers 14A and N-type extension region heavily-doped diffusion forming layers 15A having shallower junction than the pocket region of heavily-doped diffusion forming layers 14A are formed in source/drain regions of the epitaxial semiconductor substrate 11.--

On page 24, please replace the first full paragraph with the following substitute paragraph.

--In this manner, the following layers are formed: The channel diffusion layer 11a positioned below the gate electrode 13 in the epitaxial semiconductor substrate 11; extension region heavily-doped diffusion layers 15 formed from the extension region heavily-doped diffusion forming layer 15A in the semiconductor substrate 11 on both sides of the gate electrode 13 so as to sandwich the channel diffusion layer 11a; pocket region of heavily-doped diffusion layers 14 formed from the pocket region of heavily-doped diffusion forming layer 14A under the extension region heavily-doped diffusion layers 15; and the source/drain heavily-doped diffusion layers 17 formed in the semiconductor substrate 11 on both sides of the sidewall 16 and in contact with the extension region heavily-doped diffusion layers 15 and the pocket region of heavily-doped diffusion layers 14 at the side edges thereof.--

On page 24, please replace the final paragraph abridging pages 24 and 25 with the following substitute paragraph.

--In this manner, Embodiment 1 is characterized by forming the pocket region of heavily-

doped diffusion forming layer 14A in the procedure shown in FIG . 2B by implanting the heavy ions into the epitaxial semiconductor substrate 11.--

On page 26, please replace the second full paragraph with the following substitute paragraph.

--Additionally, since the In ions are implanted at a dose of 5 x $10^{13}/cm^2$ or more in forming the pocket region of heavily-doped diffusion forming layer 14A, a portion of the epitaxial semiconductor substrate 11 is changed into an amorphous layer. Therefore, in the subsequent implantation of the As ions for forming the extension region heavily-doped diffusion forming layer 15A, channeling, that is, a phenomenon that the implanted As ions penetrate between crystal lattices, can be suppressed, resulting in definitely attaining the shallow junction of the extension region heavily-doped diffusion forming layer 15A.--

On page 27, please replace the first full paragraph with the following substitute paragraph.

--Although the rapid thermal annealing is carried out after the ion implantation for forming the pocket region of heavily-doped diffusion forming layers 14A and the extension region heavily-doped diffusion forming layers 15A shown in FIG. 2B and after the ion implantation for forming the source/drain heavily-doped diffusion layers 17 shown in FIG. 2D in Embodiment 1, the rapid thermal annealing may be carried out merely in the procedure shown in FIG. 2D.--

On page 27, please replace the final paragraph abridging pages 27 and 28 with the following substitute paragraph.

--The extension region heavily-doped diffusion forming layer 15A may be formed by using another N-type dopant heavy ions having a relatively large mass number, such as antimony (Sb) ions. In this case, the Sb ions may be implanted at an acceleration energy of approximately 10 keV and a dose of approximately 2 x $10^{14}/cm^2$.--

On page 28, please replace the third full paragraph with the following substitute paragraph.

--Although the MIS transistor of Embodiment 1 is an N-channel MIS transistor, it may be a P-channel MIS transistor instead. In fabricating the P-channel MIS transistor, Sb ions are preferably used as the N-type heavy ions to be implanted for forming the channel diffusion layer 11a and the pocket region of heavily-doped diffusion forming layers 14A.--

On page 29, please replace the final paragraph abridging pages 29 and 30 with the following substitute paragraph.

--Next, as shown in FIG. 4B, with the gate electrode 33 used as a mask, P-type dopant ions such as In ions are implanted into the semiconductor substrate 31 at an acceleration energy of approximately 30 keV, a dose of approximately 1 x $10^{14}/cm^2$, a current density of approximately 100 $\mu A/cm^2$ and room temperature. Subsequently, with the gate electrode 33 used as a mask, N-type dopant ions such as As ions are implanted into the semiconductor substrate 31 at an acceleration energy of approximately 10 keV and a dose of approximately 5 x $10^{14}/cm^2$.

Thereafter, the rapid thermal annealing for increasing the temperature at a rate of approximately 100°C /sec. to a high temperature of approximately 900°C through 1025°C and keeping the temperature for approximately 1 through 10 seconds is carried out. Thus, P-type pocket region of heavily-doped diffusion forming layers 34A and N-type extension region heavily-doped diffusion forming layers 35A having shallower junction than the pocket region of heavily-doped diffusion forming layers 34A are formed in source/drain regions of the semiconductor substrate 31.--

On page 31, please replace the first full paragraph with the following substitute paragraph.

--In this manner, the following layers are formed: The channel diffusion layer 31a formed in the semiconductor substrate 31 below the gate electrode 33; extension region heavily-doped diffusion layers 35B formed from the extension region heavily-doped diffusion forming layers 35A in the semiconductor substrate 31 on both sides of the gate electrode 33 so as to sandwich the channel diffusion layer 31a; pocket region of heavily-doped diffusion layers 34B formed from the pocket region of heavily-doped diffusion forming layers 34A under the extension region heavily-doped diffusion layers 35B; and the source/drain heavily-doped diffusion layers 37 formed in the semiconductor substrate 31 on both sides of the sidewall 36 in contact with the extension region heavily-doped diffusion layers 35B and the pocket region of heavily-doped diffusion layers 34B at their side edges.--

On page 31, please replace the final paragraph abridging pages 31 and 32 with the following substitute paragraph.

--In this manner, Embodiment 2 is characterized by forming the pocket region of heavily-doped diffusion forming layer 34A by implanting the In ions at a comparatively low current density of 100 $\mu A/cm^2$ at room temperature into the semiconductor substrate 31 in the ion implantation shown in FIG. 4B. Therefore, the implantation damage caused in the semiconductor substrate 31 can be reduced by the In ions implanted at a low current density in forming the pocket region of heavily-doped diffusion forming layer 34A, and hence, formation of interstitial silicon that can be a cause of EOR dislocation loop defects can be suppressed. Accordingly, since the number of EOR dislocation loop defects caused after the annealing can be reduced, the In ions can be prevented from largely segregating in the EOR dislocation loop defect layer. As a result, a leakage current derived from the large segregation of the In ions can be suppressed.--

On page 32, please replace the first full paragraph with the following substitute paragraph.

--The current density employed in the ion implantation for forming the pocket region of heavily-doped diffusion forming layer 34A is preferably approximately 150 $\mu A/cm^2$ or less and more preferably approximately 100 $\mu A/cm^2$ or less.--

On page 32, please replace the second full paragraph with the following substitute paragraph.

--In addition, the In ions are implanted at a dose of $5 \times 10^{13}/cm^2$ or more in forming the

pocket region of heavily-doped diffusion forming layer 34A, and hence, a portion of the semiconductor substrate 31 is changed into an amorphous layer. Therefore, the channeling of the implanted As ions can be suppressed in the subsequent ion implantation of the As ions for forming the extension region heavily-doped diffusion forming layer 35A. As a result, the extension region heavily-doped diffusion forming layer 35A can definitely attain shallow junction.--

On page 33, please replace the first full paragraph with the following substitute paragraph.

--Also in Embodiment 2, the extension region heavily-doped diffusion forming layer 35A may be formed by using another N-type heavy ions having a relatively large mass number such as Sb ions. In this case, the Sb ions may be implanted at an acceleration energy of approximately 10 keV and a dose of approximately $2 \times 10^{14}/cm^2$.--

On page 33, please replace the second full paragraph with the following substitute paragraph.

--Although the rapid thermal annealing is carried out 15 after the ion implantation for forming the pocket region of heavily-doped diffusion forming layers 34A and the extension region heavily-doped diffusion forming layers 35A shown in FIG. 4B and after the implantation for forming the source/drain heavily-doped diffusion layers 37 shown in FIG. 4D in Embodiment 2, the rapid thermal annealing may be carried out merely in the procedure of FIG. 4D.--

On page 34, please replace the first full paragraph with the following substitute paragraph.

--Although the MIS transistor of Embodiment 2 is an N-channel MIS transistor, it may be a P-channel MIS transistor. In forming the P-channel MIS transistor, Sb ions are preferably used as the N-type heavy ions to be implanted for forming the channel diffusion layer 31a and the pocket region of heavily-doped diffusion forming layers 34A.--

On page 35, please replace the final paragraph abridging pages 35 and 36 with the following substitute paragraph.

--Next, as shown in FIG. 5B, with the gate electrode 43 used as a mask, P-type dopant ions such as In ions are implanted into the semiconductor substrate 41 at an acceleration energy of approximately 30 keV, a dose of approximately 1 x $10^{14}/cm^2$ and a tilt angle θ against each side face along the gate length of the gate electrode 43 of approximately 45 degrees. Subsequently, with the gate electrode 43 used as a mask, N-type dopant ions such as As ions are implanted into the semiconductor substrate 41 at an acceleration energy of approximately 10 keV and a dose of approximately 5 x $10^{14}/cm^2$. At this point, the tilt angle θ for implanting the As ions is approximately 0 through 7 degrees. Thereafter, the rapid thermal annealing for increasing the temperature at a rate of approximately 100°C /sec. to a high temperature of approximately 900°C through 1025°C and keeping the temperature for approximately 1 through 1 0 seconds is carried out. Thus, P-type pocket region of heavily-doped diffusion forming layers 44A and N-type extension region heavily-doped diffusion forming layers 45A having shallower junction than the pocket region of heavily-doped diffusion forming layers 44A are formed in source/drain

regions of the semiconductor substrate 41.--

On page 36, please replace the final paragraph abridging pages 36 and 37 with the following substitute paragraph.

--In this manner, the following layers are formed: The channel diffusion layer 41a formed in the semiconductor substrate 41 below the gate electrode 43; extension region heavily-doped diffusion layers 45B formed from the extension region heavily-doped diffusion forming layers 45A in the semiconductor substrate 41 on both sides of the gate electrode 43 so as to sandwich the channel diffusion layer 41a; pocket region of heavily-doped diffusion layers 44B formed from the pocket region of heavily-doped diffusion forming layers 44A under the extension region heavily-doped diffusion layers 45B; and the source/drain heavily-doped diffusion layers 47 formed in the semiconductor substrate 41 on both sides of the sidewall 46 in contact with the extension region heavily-doped diffusion layers 45B and the pocket region of heavily-doped diffusion layers 44B at their side edges.--

On page 37, please replace the final paragraph abridging pages 37 and 38 with the following substitute paragraph.

--In this manner, Embodiment 3 is characterized by forming the pocket region of heavily-doped diffusion forming layer 44A by implanting the In ions into the semiconductor substrate 41 at a comparatively large tilt angle of approximately 45 degrees against the side face of the gate electrode 43 in the ion implantation shown in FIG. 5B. Therefore, the implantation damage caused in the semiconductor substrate 41 can be reduced because of the In ions implanted

obliquely to the substrate surface in forming the pocket region of heavily-doped diffusion forming layer 44A. Accordingly, the formation of interstitial silicon that can be a cause of EOR dislocation loop defects can be suppressed. As a result, the number of EOR dislocation loop defects caused after the annealing can be reduced, and hence, the In ions are not strongly segregated in the EOR dislocation loop defect layer, resulting in suppressing a leakage current derived from the strong segregation of the In ions.--

On page 38, please replace the first full paragraph with the following substitute paragraph.

--The tilt angle θ employed in the ion implantation for forming the pocket region of heavily-doped diffusion forming layer 44A is preferably approximately 30 through 60 degrees and more preferably approximately 45 degrees.--

On page 38, please replace the second full paragraph with the following substitute paragraph.

--In addition, the In ions are implanted at a dose of $5 \times 10^{13}/cm^2$ or more in forming the pocket region of heavily-doped diffusion forming layer 44A, and hence, a portion of the semiconductor substrate 41 is changed into an amorphous layer. Therefore, the channeling of the implanted As ions can be suppressed in the subsequent ion implantation of the As ions for forming the extension region heavily-doped diffusion forming layer 45A. As a result, the extension region heavily-doped diffusion forming layer 45A can definitely attain shallow junction.--

On page 39, please replace the first full paragraph with the following substitute paragraph.

--Also in Embodiment 3, the extension region heavily-doped diffusion forming layer 45A may be formed by using another N-type heavy ions having a relatively large mass number such as Sb ions. In this case, the Sb ions may be implanted at an acceleration energy of approximately 10 keV and a dose of approximately $2 \times 10^{14}/cm^2$.--

On page 39, please replace the second full paragraph with the following substitute paragraph.

--Although the rapid thermal annealing is carried out after the ion implantation for forming the pocket region of heavily-doped diffusion forming layers 44A and the extension region heavily-doped diffusion forming layers 45A shown in FIG. 5B and after the implantation for forming the source/drain heavily-doped diffusion layers 47 shown in FIG. 5D in Embodiment 3, the rapid thermal annealing may be carried out merely in the procedure of FIG. 5D.--

On page 39, please replace the final paragraph abridging pages 39 and 40 with the following substitute paragraph.

--Although the MIS transistor of Embodiment 3 is an N-channel MIS transistor, it may be a P-channel MIS transistor. In forming the P-channel MIS transistor, Sb ions are preferably used as the N-type heavy ions to be implanted for forming the channel diffusion layer 41a and the pocket region of heavily-doped diffusion forming layers 44A.--

On page 40, please replace the final paragraph abridging pages 40 and 41 with the following substitute paragraph.

--In an upper portion of the <110> semiconductor substrate 51, source/drain heavily-doped diffusion layers 57 where N-type As ions are diffused are formed in source/drain regions on both sides of a sidewall 56 of the gate electrode 53 at a distance from a region below each side face of the gate electrode 53. Between the source/drain heavily-doped diffusion layer 57 and the region below the side face of the gate electrode 53, an extension region heavily-doped diffusion layer 55 where N-type As ions are diffused to have shallower junction than the source/drain heavily-doped diffusion layer 57 is formed, and under the extension region heavily-doped diffusion layer 55, a pocket region of heavily-doped diffusion layer 54 where P-type In ions, that is, heavy ions having a relatively large mass number, are diffused is formed.--

On page 41, please replace the first full paragraph with the following substitute paragraph.

--Furthermore, in a portion of the <110> semiconductor substrate Si below the gate electrode 53 and sandwiched between the extension region heavily-doped diffusion layers 55 and between the pocket region of heavily-doped diffusion layers 54, a channel diffusion layer 51a where P-type In ions are diffused is formed.--

On page 41, please replace the second full paragraph with the following substitute paragraph.

--In this manner, the MIS transistor of this embodiment is characterized by including the pocket region of heavily-doped diffusion layer 54 where the In ions, that is, the heavy ions, are diffused in the <110> semiconductor substrate 51.--

On page 41, please replace the third full paragraph with the following substitute paragraph.

--In FIG. 6B, a curve 1C indicates an As ion concentration in the extension region heavily-doped diffusion layer 55 and a curve 2C indicates an In ion concentration in the pocket region of heavily-doped diffusion layer 54. A curve 3 indicates, for a comparison, an In ion concentration in a pocket region of heavily-doped diffusion layer formed in a semiconductor substrate of a general silicon wafer having a <100>-oriented zone axis.--

On page 42, please replace the first full paragraph with the following substitute paragraph.

--In the semiconductor fabrication process, a heavy ion having a relatively large mass number such as an In ion exhibits abrupt and shallow profile as compared with an ion having a relatively small mass number such as a boron (B) ion. In addition, as shown in FIG. 6B, the heavy ions are less diffused in a tale portion with a low concentration in the dopant profiled namely, in a deep region, owing to segregation in a defect layer or surface diffusion. Therefore, an abrupt profile can be realized in not only the curve 1C of the dopant concentration of the extension region heavily-doped diffusion layer 55 but also the curve 2C of the dopant concentration of the pocket region of heavily-doped diffusion layer 54. As a result, even in a MIS transistor with a small gate length, shallow junction can be obtained, so as to realize high

driving power. Furthermore, since the extension region heavily-doped diffusion layer 55 and the pocket region of heavily-doped diffusion layer 54 can be formed with shallow junction, the short channel effect can be suppressed, and hence, a fine transistor can be designed.--

On page 43, please replace the first full paragraph with the following substitute paragraph.

--As a result, as understood from FIG. 6B, the number of EOR dislocation loop defects is smaller in the dopant curve 2C of the pocket region of heavily-doped diffusion layer 54 of this embodiment than in the dopant curve 3 of the pocket region of heavily-doped diffusion layer formed in the conventional <100> semiconductor substrate, and the peak of a segregation portion of the In ions in the EOR dislocation loop defect layer is lowered. Also, a leakage current derived from the EOR dislocation loop defects can be suppressed.--

On page 44, please replace the final paragraph abridging pages 44 and 30 with the following substitute paragraph.

--Next, as shown in FIG. 7B, with the gate electrode 53 used as a mask, P-type dopant ions such as In ions are implanted into the <110> semiconductor substrate 51 at an acceleration energy of approximately 30 keV and a dose of approximately 1 x $10^{14}/cm^2$. Subsequently, with the gate electrode 53 used as a mask, N-type dopant ions such as As ions are implanted into the <110> semiconductor substrate 51 at an acceleration energy of approximately 10 keV and a dose of approximately 5 x $10^{14}/cm^2$. Thereafter, the rapid thermal annealing for increasing the temperature at a rate of approximately 100°C /sec. to a high temperature of approximately 900°C

through 1025°C and keeping the temperature for approximately 1 through 1 0 seconds is carried out. Thus, P-type pocket region of heavily-doped diffusion forming layers 54A and N-type extension region heavily-doped diffusion forming layers 55A with shallower junction than the pocket region of heavily-doped diffusion forming layers 54A are formed in source/drain regions of the <110> semiconductor substrate 51.--

On page 46, please replace the final paragraph abridging pages 46 and 47 with the following substitute paragraph.

--In this manner, Embodiment 4 is characterized by forming pocket region of heavily-doped diffusion forming layer 54A by implanting heavy ions into <110> semiconductor substrate 51 in the procedure shown in FIG. 7B. Therefore, the implanted In ions minimally collide with the silicon crystal lattice because of the channeling of the implanted In ions as described above, and hence, the implantation damage caused in the silicon crystal lattice by the In ions is reduced, so as to reduce the formation of interstitial silicon that can be a cause of EOR dislocation loop defects. At this point, even though the implanted In ion is channeled, the implantation range is not largely increased due to the mass effect of In as compared with that of another light ion. Since the implantation damage caused by the In ions is thus reduced, the interstitial silicon that can be a cause of the EOR dislocation loop defects is reduced, and hence, the formation of the EOR dislocation loop defect layer is suppressed, resulting in reducing the In ions segregated in the EOR dislocation loop defect layer. As a result, the pocket region of heavily-doped diffusion layer 54 can be formed by using the heavy ions without increasing a leakage current.

On page 47, please replace the first full paragraph with the following substitute paragraph.

--In addition, even though the implantation damage caused by the In ions is reduced, since a portion of the <110> semiconductor substrate 51 is changed into an amorphous layer, the implantation of the As ions for forming the extension region heavily-doped diffusion forming layer 55A carried out after the pocket implantation of the In ions is conducted on the amorphous silicon layer. Therefore, a pre-amorphous effect works. Accordingly, the channeling of the As ions used for the extension implantation can be suppressed, so that the extension region heavily-doped diffusion layer 55 can be formed to have very shallow junction.--

On page 48, please replace the first full paragraph with the following substitute paragraph.

--Although the rapid thermal annealing is carried out after the ion implantation for forming the pocket regions of heavily doped diffusion forming layers 54A and the extension regions heavily-doped diffusion forming layers 55A shown in FIG. 7B and after the implantation for forming the source/drain heavily-doped diffusion layers 57 shown in FIG. 7D in Embodiment 4, the rapid thermal annealing may be carried out merely in the procedure of FIG. 7D.--

On page 48, please replace the second full paragraph with the following substitute paragraph.

--Also in Embodiment 4, the extension region heavily-doped 20 diffusion forming layer

55A may be formed by using another N-type heavy ions having a relatively large mass number such as Sb ions. In this case, the Sb ions may be implanted at an acceleration energy of approximately 10 keV and a dose of approximately 2 x $10^{14}/cm^2$.--

On page 49, please replace the second full paragraph with the following substitute paragraph.

--Although the MIS transistor of Embodiment 4 is an N-channel MIS transistor, it may be a channel MIS transistor. IN forming the P-channel MIS transistor, Sb ions are preferably used as the N-type heavy ions to be implanted for forming the channel diffusion layer 51a and the pocket regions of heavily-doped diffusion forming layers 54A.--